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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/577,173	10/27/2009	Wolfgang Hetzel	I441.141.101	1239
73158	7590	09/03/2010	EXAMINER	
Dicke, Billig, & Czaja, PLLC 100 South 5th Street, Suite 2250 Minneapolis, MN 55402			MITCHELL, JAMES M	
			ART UNIT	PAPER NUMBER
			2813	
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/577,173	HETZEL ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	JAMES M. MITCHELL	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 26 April 2006.  
 2a) This action is **FINAL**.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 16-35 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 16-30 and 32-35 is/are rejected.  
 7) Claim(s) 31 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>4/26/06, 6/17/09</u> .	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____ .

## **DETAILED ACTION**

1. This office action is in response to the application filed April 26, 2006.

### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on April 26, 2006 and June 17, 2009 was in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### ***Specification***

3. Claim 34 is objected to because of the following informalities: the claim appears incomplete. Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 34 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim is either missing or incomplete. Failure to include a preamble makes it unclear as to if applicant is claiming for example a method or product claim.

### ***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 16-23, 26-30, 32 and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by Moden (U.S 6,310,390)<sup>1</sup>.

8. Moden (Fig. 1C) discloses

(cl. 16, 19, 35) A semiconductor device comprising: a plastic package molding compound (18); a semiconductor chip (12); a leadframe (14), the semiconductor chip being embedded in the plastic package molding compound (e.g. Fig. 1C) are arranged on the leadframe, and a continuous elastic adhesive layer (36 not separated in pieces but integral) being arranged between the plastic package molding compound and the leadframe (e.g. molding over a portion of adhesive), and between the semiconductor chip and the leadframe;

(cl. 17, 20, 28) peripheral regions of the semiconductor device are free of the elastic adhesive layer (e.g. 36 not on top or sides of 12);

(cl. 18, 21, 29) peripheral regions of the semiconductor device are free of the elastic adhesive layer comprise elastic metal layers (30);

(cl. 22) the metal layers (e.g. alternatively part of leads) comprise a copper layer of a copper alloy arranged on the leadframe and a gold layer of a gold alloy applied on top of it (Col. 4, Lines 52-59);

(cl. 23) the metal layers comprise a copper layer of a copper alloy arranged on the leadframe and a gold layer of a gold alloy applied on top of it (Col. 4, Lines 52-59);

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<sup>1</sup> Note even if applicant amends the claims that elastic adhesive covers the entire leadframe it still would be obvious in light of Courtenay in combination with Moden that could have been used to anticipate or make obvious the claimed invention showing use or an elastic polyimide over and between entire leadframes and chips.

(cl. 27) A panel, comprising device positions with semiconductor devices arranged in rows and columns, as claimed in claim 16 (Fig. 2D, 3).

(c. 30) A method for producing a panel with a plastic package molding compound, semiconductor chips and a leadframe in a number of semiconductor device positions, the method comprising: producing a leadframe with device positions arranged in rows and/or columns (44; Fig. 2D, 3); applying an elastic adhesive layer (36), covering both the region of the intended semiconductor chip and the region of the intended plastic package molding compound on an upper side of the leadframe in the device positions (Fig. 1C); adhesive attachment of semiconductor chips onto the adhesive layer in the device positions (e.g. chip on adhesive); establishing electrical connections (30) between contact areas of the semiconductor chip and the leadframe in the device positions; and applying a plastic package molding compound (48) to the adhesive layer while embedding the semiconductor chips and while forming a panel with a number of semiconductor device positions;

(cl. 32) wherein a central opening for a bonding channel (e.g. space between leads and die pad) is introduced in the device positions of the leadframe when the leadframe is produced;

(cont. cl. 35) and means (e.g. conventional die attacher Col. 5, Lines 22-25; )for providing an elastic adhesive layer arranged between the plastic package molding compound and the leadframe, and between the semiconductor chip and the leadframe, on the upper side of the leadframe.

9. With respect to the) intended use limitation of claim 16 that configured for mechanical decoupling of an upper region from a lower region of the semiconductor device, the prior art forms the same structure as claimed by applicants and therefore performs in the same manner. See e.g. *Ex parte Masham*, 2 USPQ2d 1647 (1987) (held that the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations.)

10. With respect to the process limitation of claims 26 and 34 that the width of the metal layers in the peripheral regions of the semiconductor device are adapted to the width of sawing tracks in such a way that the elastic adhesive layer is not exposed to the sawing process (e.g. 36 not in sawing region; Fig. 3) in the production of peripheral sides of the semiconductor device, it does not impart patentability since the prior art forms the same structure as claimed. “[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process.” In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985)

***Claim Rejections - 35 USC § 103***

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moden (U.S 6,310,390)

13. Moden discloses the elements stated in paragraphs 8-10 of this office action, but does not disclose its leadframe comprising silver layer of a silver alloy applied on top of copper.

14. Examiner takes official notice that use of silver over copper is known in the art for forming leadframes. As such the selected material would have been obvious to one of ordinary skill in the art, since it has been held that the selection of a known material based on its suitability for its intended use supported a *prima facie* obviousness determination in *Sinclair & Carroll Co. v. Interchemical Corp.*, 325 U.S. 327, 65 USPQ 297 (1945).

15. With respect to claim 25 see paragraph 10 of this office action.

16. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moden (U.S 6,310,390) in combination with Grigg et al. (U.S. 2002/0030253).

17. Moden discloses the elements stated in paragraphs 8-10 of this office action, but does not disclose semiconductor chip is applied with its active upper side to the adhesive layer of the leadframe while aligning contact areas of the semiconductor chip arranged in two rows over the central opening of the leadframe, and bonding wires for connecting the contact areas of the semiconductor chip to bonding fingers of a wiring

structure are attached on the rear side of the leadframe in the device positions.

18. Grigg disclose its semiconductor chip (34) applied with its active upper side to the adhesive layer (40) of the leadframe (14) while aligning contact areas of the semiconductor chip arranged in two rows over the central opening of the leadframe, and bonding wires for connecting the contact areas of the semiconductor chip to bonding fingers of a wiring structure are attached on the rear side of the leadframe in the device positions (Fig. 4).

19. It would have been obvious to one of ordinary skill in the art to modify the conventional wirebond of Ma with the LOC of Grigg in order to assist in heat dissipation and provide convenient locations for eletrical contact as taught by Grigg (Par. 0006).

#### ***Allowable Subject Matter***

20. Claim 31 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

21. The following is a statement of reasons for the indication of allowable subject matter: a pattern of metal layers, which covers more than the width of the sawing tracks with the metal layers, and having a width in the range of 1.2 times to 3 times the width of the sawing tracks, is applied to the leadframe before the application of the adhesive layer including all the limitations of the independent claim.

#### ***Conclusion***

22. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses in: Li et al. (U.S 7, 012.324) and Grigg et al. (U.S 2002/0030253) use of elastic adhesive between frame and chip; Takahashi (U.S. 5, 059,559) polyimides being elastic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES M. MITCHELL whose telephone number is (571)272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 30, 2010  
/James M. Mitchell/  
Examiner, Art Unit 2813

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